

REMARKS

In the Office Action of November 28, 2007, the Examiner (1) rejected claim 9 under 35 U.S.C. § 103(a) as allegedly obvious over U.S. Patent No. 6,041,399 ("Terada") in view of U.S. Patent No. 5,659,722 ("Blaner"), and in view of *The SPARC Architecture Manual: Version 9* ("Weaver"); (2) rejected claim 10 as allegedly obvious over Terada in view of Blaner, in view of Weaver, further in view of U.S. Patent No. 5,504,903 ("Chen et al."); (3) rejected claims 1, 3, 5, 8, and 21 as allegedly obvious over Terada, in view of U.S. 6,931,632 ("Ramasamy et al."), in view of Blaner, in view of Weaver; (4) rejected claims 11, 13, 15, 18, and 22 as allegedly obvious over Terada in view of Patent No. 6,088,786 ("Feierbach et al."), in view of Blaner, in view of Weaver; and (5) rejected claims 19-20 as allegedly obvious over Terada, in view of Ramasamy, in view of U.S. Patent No. 5,638,525 ("Hammond et al."), in view of Blaner, in view of Weaver. Based on the amendments and arguments presented herein, Applicants respectfully request reconsideration and allowance of the pending claims.

Claim 1 requires a single instruction capable of performing two different types of comparison operations based on the status of a bit which is not part of the opcode. The Examiner has been forced to reject claim 1 over the combination of no less than four references. According to the Examiner:

- Terada teaches one of the claimed types of comparison;
- Ramasamy teaches a jump to another routine;
- Blaner teaches the other type of comparison; and
- Weaver teaches a control bit.

Thus, while the Examiner has not found any one reference that teaches the specific combination of limitations of claim 1, the Examiner has allegedly found each limitation in one of four different prior art references. As the Examiner is no doubt aware, an obviousness rejection cannot be based on hindsight gleaned from the inventor's own teachings. Further, the CAFC has emphasized this point. "This is essential for combination inventions, for generally all combinations are of known elements."

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Interconnect Planning Corp. v. Feil, 774 F.3d 1132, 1143 (Fed. Cir. 1985). Applicants submit that, absent the hindsight of Applicants' own specification, one of ordinary skill in the art would not have been motivated to seek out and combine the four references used by the Examiner.

Further, the Examiner seems to have analogized Weaver's "rcond" field to the claimed "bit". Weaver teaches that the rcond field is a "3-bit field [that] selects the register-contents condition to test for a move based on register contents (MOVr or FMOVr) instructions or a branch on register contents with prediction (BPr) instruction." This teaching is not of a bit "specifies whether the register reference is to a register from a first group of registers or to a register from a second group of registers" as is required by claim 1. If the bit specifies a register from the first group, the comparison is performed by comparing the immediate value to the register value, and, if to the second group, the comparison is performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register. The rcond field of Weaver does not provide this functionality. Even if one were to combine Weaver's rcond field with the teachings of Terada, Ramasamy and Blaner, one still would not have the invention of claim 1.

For at least this reason, claim 1 and all claims dependent thereon are in condition for allowance. For much the same reason, all other claims are in condition for allowance.

Claims 21 and 22 require an assessment of whether the masked version of the register is all high/low values or a mix of high and low values. The Examiner used Blaner for this teaching, but acknowledged that Blaner does not specifically teach this limitation. The Examiner noted that Blaner teaches the use of AND and OR gates, but concluded that it would have been obvious to use an exclusive NOR (XNOR) gate. An XNOR gate outputs a high if the input values are all 0 or all 1, otherwise a logic low is output (mix logic inputs). Applicants respectfully request the Examiner to justify why he believes this specific limitation would have been obvious even though the cited art admittedly does not teach it. Further, absent hindsight from Applicants' specification (which cannot be used),

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Applicants do not see that one of ordinary skill in the art would have been motivated to use an XNOR gate in Blaner. For this additional reason, claims 21 and 22 are allowable.

CONCLUSION

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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